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FMDRX , H4T TABE TABF TADD
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# (54) Switch mode power supply controller

(57) A controller for a switch mode power supply in a television receiver or computer display comprises a first oscillator (4) generating a first pulse signal (11), for actuating a switching device (Q1). A pulse width modulation feedback signal (12) indicative of a load on the power supply varies the pulse width of the first pulse signal (11) as a function of the feedback signal. A second oscillator (1) generates a second pulse signal for actuating the switching device (Q1). The second pulse signal is of a lower frequency than the first pulse signal. A multiplexor (2) selectively supplies one of the first pulse signal and the second pulse signal to the switching device (Q1) in response to a control signal (10) to configure the switch mode power supply to operate in a corresponding one of a higher power normal operating mode or a lower power standby mode.

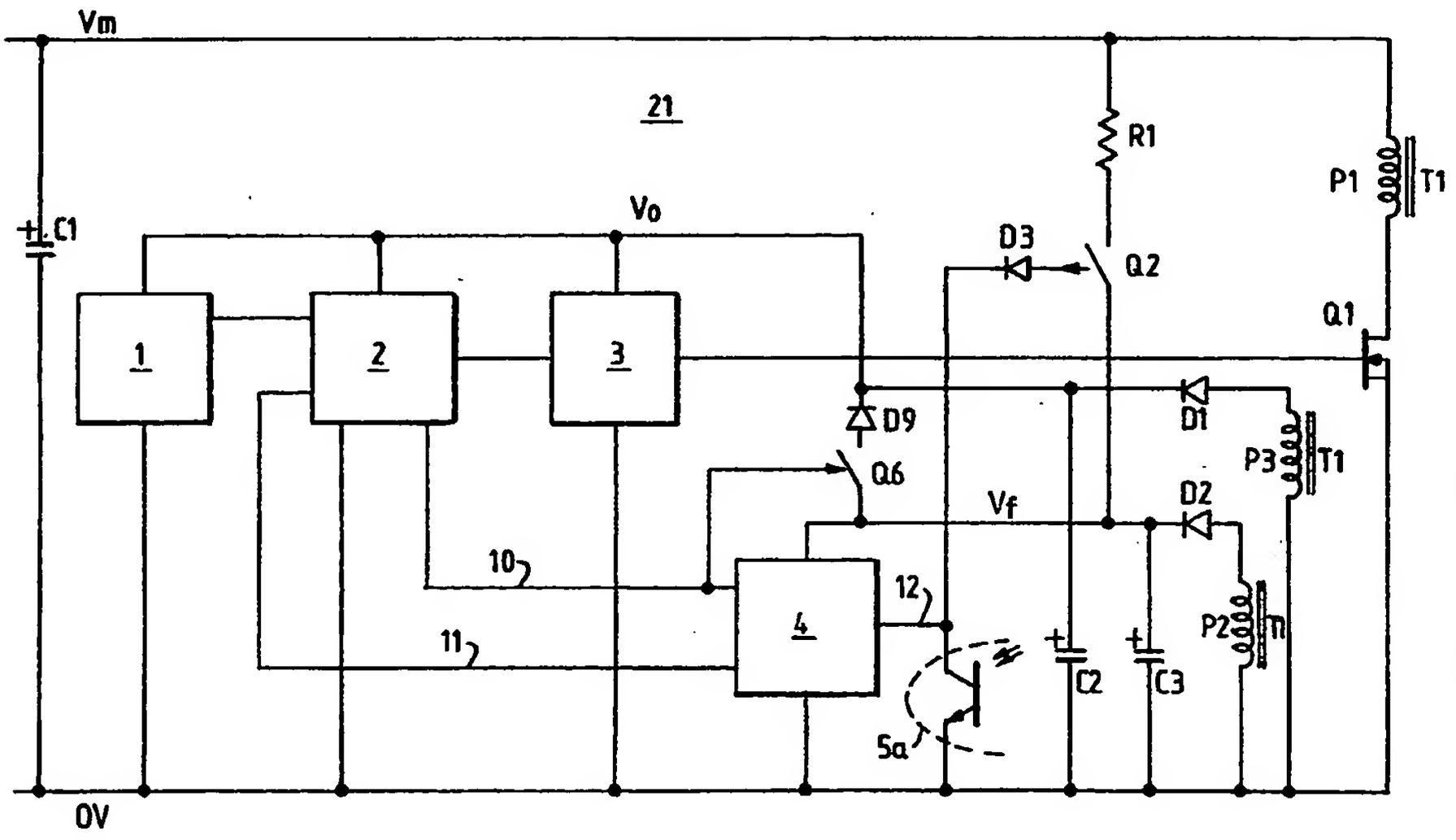


FIG. 2

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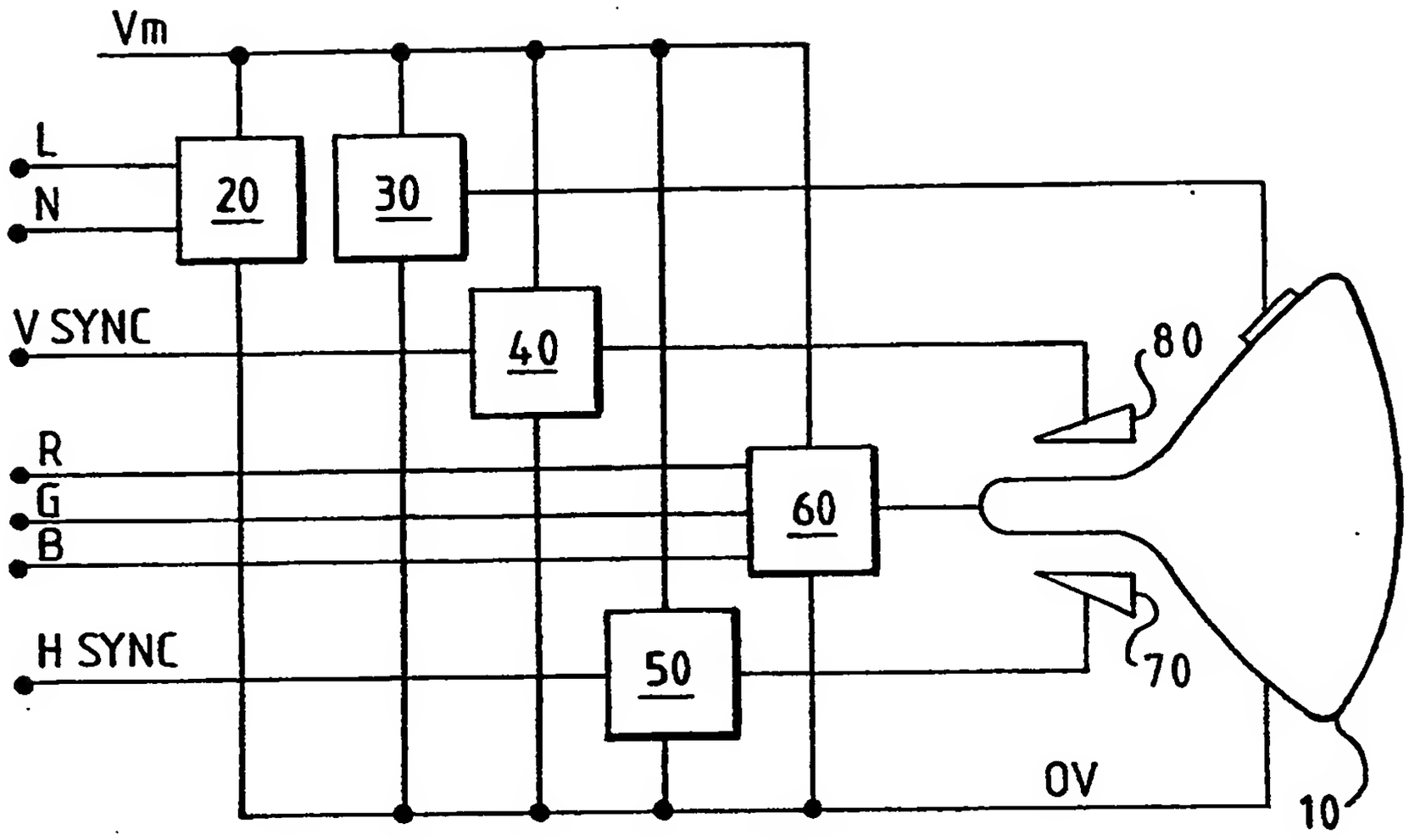


FIG. 1

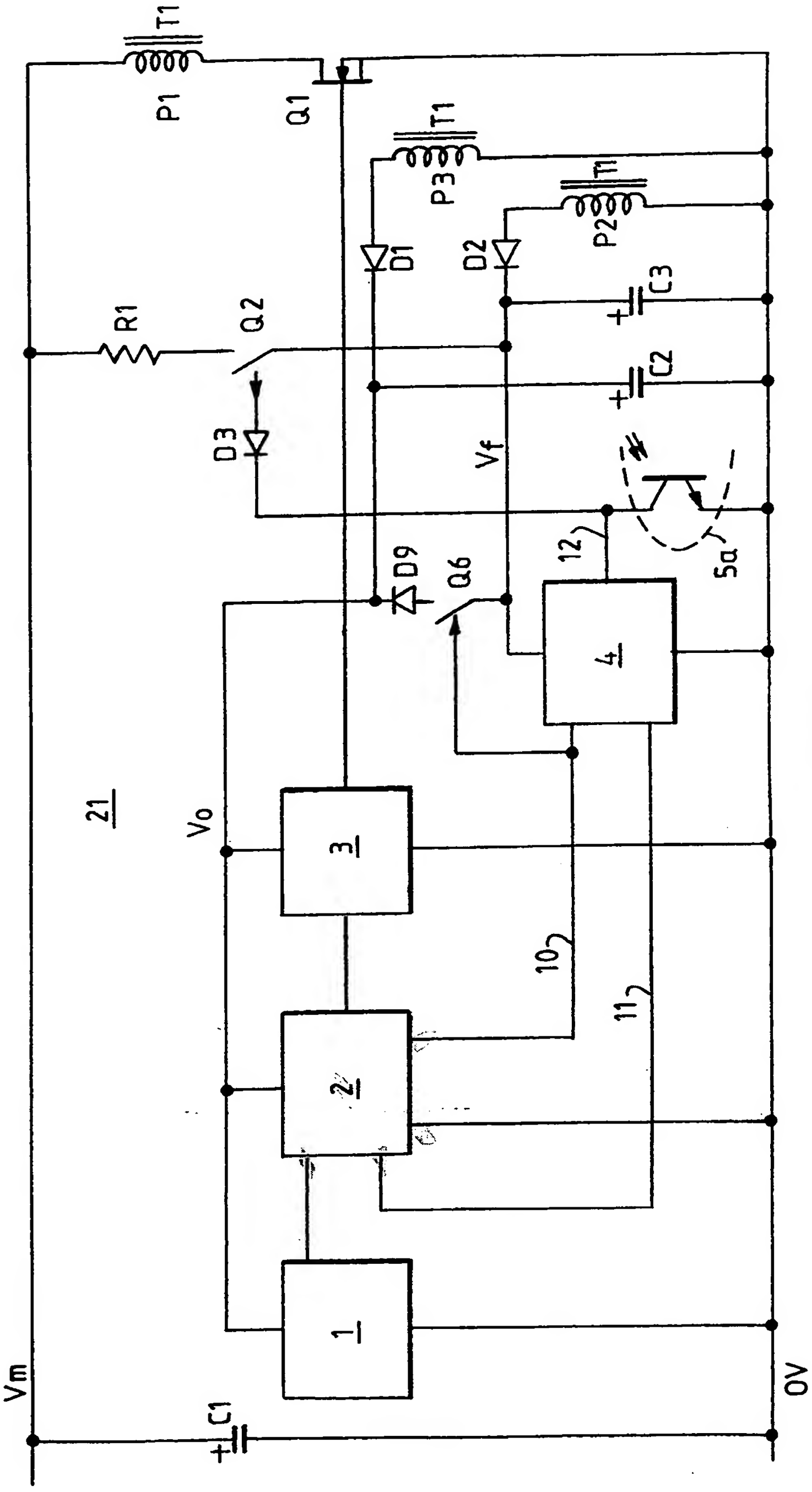
T1
P1
Q1
T1
P3
T1
P2
D1
D2
C3
R1
Q2
C2
D3
Vf
12
5a
D9
Q6
4
21
Vo
3
10
11
2
1
Vm
C1
0V

FIG. 2

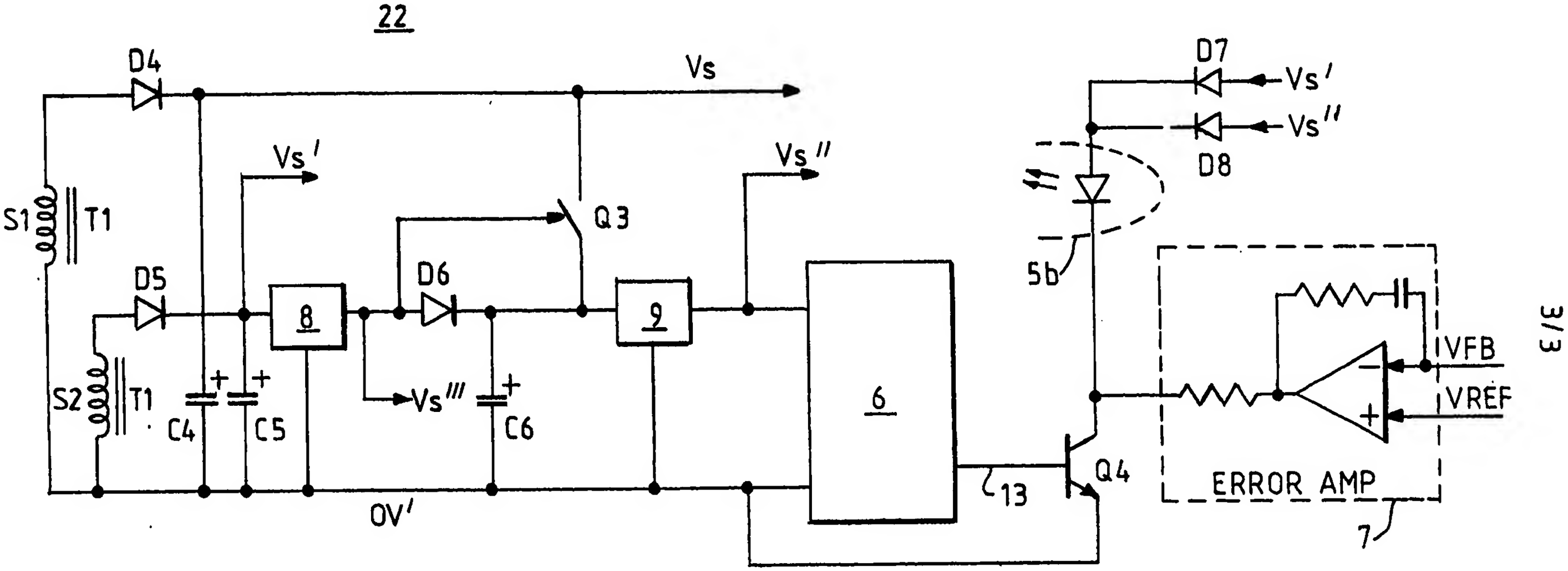
22
D4
Vs
Vs'
Vs''
S1
T1
Q3
D5
D6
8
9
6
D7
Vs'
Vs''
D8
5b
S2
T1
C4
C5
Vs'''
C6
OV'
13
Q4
VFB
VREF
ERROR AMP
7

FIG. 3

# SWITCH MODE POWER SUPPLY CONTROLLER

## DESCRIPTION

The present invention relates to a switch mode power supply controller for generating a switching signal in a switch mode power supply (SMPS).

Switch mode power supplies, or DC to DC convertors as they are sometimes referred to, are used in electrical appliances, such as television receivers and computer visual display units for example, to efficiently transfer electrical power from the domestic electricity mains supply to electrical circuitry of the appliances.

A typical SMPS comprises a switch for alternately opening and closing a current path through the primary winding of a transformer in response to a square wave switching signal. In operation, a DC voltage is applied across the primary winding of the transformer. Electrical energy is transferred to a load connected to the secondary winding of the transformer by alternately opening and closing the switch as a function of the switching signal. The amount of electrical energy transferred to the load is a function of the duty cycle of the switch and the frequency of the switching signal. The duty cycle of the switch is the ratio of the time for which the switch is open relative to the time for which the switch is closed. The duty cycle thus corresponds to the mark-space ratio of the switching signal.

A switch mode power supply controller typically comprises an oscillator for generating the switching signal. A pulse width modulator is connected to the output of the oscillator for varying the mark-space ratio of the switching signal to vary the duty cycle of the switch as a function of a feedback signal from the load. The feedback signal from the load completes a negative feedback loop enabling the controller to regulate the power supplied to the load in accordance with the power demanded by the load, thereby leading to efficient energy usage.

EP 255 839 describes a switch mode power supply controller for a cathode ray tube (CRT) television receiver which can be switched to stand-by operation. The oscillator of the controller is synchronised to a raster line frequency of at least 15kHz corresponding to the received television transmission. In normal operation, the switching signal is provided directly from the output of the oscillator to operate the switch at the line frequency of the received TV transmission. In standby operation, the switching signal is generated by gating the output of the oscillator through a frequency divider circuit to operate the switch at half the line frequency. The power transferred to the load during standby operation is thus reduced. However, if the raster line frequency is less than 40kHz, the divider will place the frequency of the switching signal in the audible range. The host power supply may therefore generate undesirable audio noise when in stand-by operation. Furthermore, the pulse width from the divider circuit cannot readily be tuned to bring the television receiver into line with both existing and emerging international and national government and industry standards.

In accordance with the present invention, there is now provided a controller for a switch mode power supply, the controller comprising: a first oscillator for generating a first pulse signal for actuating a switching device of the power supply, the first pulse signal having a first frequency; and a pulse width modulator for receiving a feedback signal indicative of a load on the power supply and for varying the pulse width of the first pulse signal generated by the first oscillator as a function of the feedback signal; characterised in that the controller comprises: a second oscillator for generating a second pulse signal having a second frequency for actuating the switching device, the second pulse signal having a second frequency lower than the first frequency; and a multiplexor for selectively supplying one of the first pulse signal and the second pulse signal to the switching device in response to a control signal to configure the switch mode power supply to operate in a corresponding one of a higher power normal operating mode or a lower power standby mode.

Because, in accordance with the present invention, the second pulse signal is generated by a second oscillator independently of the first oscillator, the second pulse signal can be set any frequency and pulse width required to provide adequate power to sustain standby operation of the host appliances and to simultaneously meet with national and international government and industry standards such as, for example, NUTEK Specification 803299.

Preferably, the frequency of the second pulse signal generated by the second oscillator is greater than 20kHz to avoid generation of audio noise when operating in standby mode.

In a preferred embodiment of the present invention the pulse width of the second pulse signal generated by the second oscillator is less than 1us. The frequency of the first pulse signal may be in the range 30kHz to 100kHz.

It will be appreciated from the following that the present invention extends to a switch mode power supply, comprising: a transformer having a primary winding and at least one secondary winding; a switching device connected to the primary winding of the transformer; and a controller as described above connected to the switching device, the feedback signal being derived from the secondary winding of the transformer.

It will also be appreciated from the following that the present invention extends to display apparatus comprising drive means for driving a display device in response to one or more video signals, processor means for controlling the drive means and a switch mode power supply as described above.

A preferred embodiment of the present invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a CRT display device;

Figure 2 is a block diagram of th primary side of a switch mode power supply including a controller of the present invention; and

Figure 3 is a block diagram of the secondary side of the switch mode power supply.

Referring first to Figure 1, a CRT display, such as a computer visual display unit or a television receiver for example, comprises a Cathode Ray Tube (CRT) 10 connected to an Extra High Tension voltage (EHT) generator 30 and a video amplifier 60. Line and frame deflection coils, 80 and 70 respectively, are disposed around the neck of the CRT 10. Deflection coils 80 and 70 are connected to line and frame scan circuits, 40 and 50, respectively. A switch mode power supply (SMPS) 20 is connected via power supply rails Vin and 0V to the EHT generator 30, video amplifier 60 and scan circuits 40 and 50.

In operation, EHT generator 30 generates an electric field within CRT 10 for accelerating electrons in beams towards the screen of CRT 10. Line and frame scan circuits 40 and 50 generate line and frame scan currents in deflection coils 70 and 80. The line and frame scan currents are in the form of ramp signals to produce time-varying magnetic fields that scan the electron beams across CRT screen 10 in a raster pattern. The line and frame scan signals are synchronised by line and frame scan circuits 50 and 40 to input line and frame sync signals, HSYNC and VSYNC, generated by a host computer system (not shown) for example. Video amplifier 60 modulates the electron beams to produce an output display on CRT 10 as a function of input video signals, R,G and B, also generated by the host computer system.

Referring to Figures 2 and 3 together, SMPS 20 comprises a primary side 21 and a secondary side 22 linked by a transformer T1. The primary side of SMPS 20 has flyback switching topology. T1 comprises a primary winding P1, a flyback winding P2, a forward winding P3, and secondary windings S1 and S2.

The primary winding is connected at one end via a DC input rail Vm to a bulk storage capacitor C1 and at the other end to the drain of a field effect transistor (FET) switch Q1. It will be appreciated from the following that, in other embodiments of the present invention Q1 may be implemented by a bipolar transistor instead of a FET. The source of Q1 is connected a reference rail 0V. The gate of Q1 is connected to the output 14 of a driver amplifier 3. The input to driver 3 is connected to the output of a two input multiplexor 2. In accordance with the present invention, one input of multiplexor 2 is connected to the output of an oscillator 1. The other input to multiplexor 2 is connected to a switching signal output 11 of a control device 4. A control output 10 of control device 4 is connected to control inputs of multiplexor 2 and driver 3. A feedback input 12 to control device 4 is connectable to 0V via the output transistor 5a of an opto-isolator. Feedback input 12 is also connected via a reverse-biased diode D3 to the control input of a switch Q2. DC input rail Vm is connectable to a supply input Vf to control device 4 via a resistor R1 and a switch Q2. Supply input Vf to control device 4 is also connectable via a switch Q6 and a diode D9 to a supply rail Vo. Supply rail Vo is connected via a diode D1 to forward winding P3. Control device 4 contains an oscillator (not shown) for generating a pulse signal synchronised to the line scan signal generated by line scan circuit 50, and a pulse width modulator (not shown) connected to the output of the oscillator. The pulse width modulator has a modulation input connected to feedback input 12 of control device 4. The output of the pulse width modulator is connected to switching signal output 11 of control device 4.

In operation, DC input rail Vm carries DC-rectified mains power smoothed by bulk storage capacitor C1. The DC rectified mains power is supplied, via a bridge rectifier (not shown) from the domestic electricity mains power supply. Initially, Q2 is closed and supply input Vf to control device 4 is connected to DC input rail Vm through R1. Control device 4 therefore initially receives power from DC input rail Vm.

The oscillator of control device 4 starts up in response to the power supplied via R1 to generate a switching signal on output 11. Control output

10 is sent high by the power supplied to control device 4 via R1. Q6 is closes in response to control output 10 going high. Therefore, power to driver 3 and multiplexor 2 is initially supplied from supply input Vf via supply rail Vo and diode D9. Multiplexor 2 gates the switching signal via driver 3 onto the gate of Q1 in response to control output 10 going high. Driver 3 conditions the switching signal for application to the gate of Q1. In response to the switching signal, Q1 alternately opens and closes the current path from DC rail Vm to 0V. Electrical energy is thus transferred to second side 22 of SMPS 20 by flyback action. Transistor 5a of opto-isolator starts to conduct in response to power demand from second side 22 of SMPS 20, thereby opening switch Q2. However, power to control device 4 is now maintained also by flyback action on voltage rail Vf via flyback winding P2, a rectifier diode D2, and a smoothing capacitor C3. However, power to driver 3, multiplexor 2, and oscillator 1 is now provided by transformer action on voltage rail Vo via forward winding P3, rectifier diode D1 and smoothing capacitor C2. Transistor 5a of the opto-isolator generates a feedback signal on feedback input 12 as a function of the demand from secondary side 22 of SMPS 20. The pulse width modulator of control device 4 varies the pulse width of the switching signal at output 11 as a function of the feedback signal. Transistor switch Q1 is alternately turned on and off by the pulse width modulated switching signal in accordance with the energy demand from secondary side 22 of SMPS 20. Initially the oscillator of control device 4 generates the switching signal at a free-running frequency. However, once normal power is supplied to secondary side 22 of the SMPS 20, the oscillator synchronises the switching signal to line sync signal HSYNC input to the CRT display. The frequency of line sync signal HSYNC is typically in the range 32kHz to 64kHz.

Secondary winding S1 is connected at one end via rectifier diode D4 to a high voltage power supply rail Vs and at the other end to a secondary side reference level 0V'. A smoothing capacitor C4 is connected between the cathode of D4 and reference level 0V'. In operation, supply rail Vs carries a DC voltage of about 75V relative to reference level 0V', rectified by D4 and smoothed by C4, to high voltage portions of line scan circuit 50, video amplifier 60, and EHT generator 30.

Secondary winding S2 is connected at one end via a rectifier diode D5 to a low voltage supply rail Vs' and at the other end to reference level 0V'. A smoothing capacitor C5 is connected between the cathode of D5 and reference level 0V'. Supply rail Vs' is also connected to the input of a voltage regulator 8 referenced to reference level 0V'. In operation, supply rail Vs' carries a DC voltage of about 16V relative to reference level 0V', rectified by D5 and smoothed by C5, to frame scan circuit 40. The output of regulator 8 is connected to another low voltage supply rail Vs'''. In operation, voltage regulator 8 sets the voltage on supply rail Vs''' to a fraction of that on supply rail Vs' relative to reference level 0V'. Supply rail Vs''', in use, carries a DC voltage of about 12V to low voltage portions of frame scan circuit 40, line scan circuit 50, video amplifier 60, and EHT generator 30. The output of voltage regulator 8 is also connected via a rectifier diode D6 to the input of another voltage regulator 9 referenced to reference level 0V'. A capacitor C6 is connected between the input of voltage regulator 9 and reference level 0V' to smooth the voltage at the input to voltage regulator 9. The output of voltage regulator 9 is connected to a very low voltage supply rail Vs''. In operation, voltage regulator 8 sets the voltage on supply rail Vs'' to a fraction of that on supply rail Vs''' relative to reference level 0V'. Supply rail Vs'', in use, carries a DC voltage of about 5V to a processor logic 6 in the form of a microprocessor for controlling the operation of frame scan circuit 40, line scan circuit 50, video amplifier 60, and EHT generator 30.

In accordance with the present invention, supply rail Vs is connectable to the input of voltage regulator 9 via a switch Q3 having a control input connected to the output of voltage regulator 8. Supply rails Vs' and Vs'' are connectable to reference level 0V' via respective diodes D7 and D8, a light emitting diode (LED) 5b of the opto-isolator, and a switch in the form of a bipolar transistor Q4 having a base connected to a shutdown output 13 of processor 6. The output of an error amplifier 7 is connected to the collector of Q4. Error amplifier 7 has a positive input connected to receive in operation a referenc  voltage VREF and a negative input connected to a feedback source in the form of the output a line scan

signal regulator (not shown) of line scan circuit 50. The line scan regulator of line scan circuit 50 operat s to maintain constant picture width despite changes in line scan frequency resulting form, for example, the CRT display being switched from one display format to the other. In operation, the line scan regulator outputs a voltage VFB indicative of the energy demanded from supply rail Vs by line scan circuit 50. The output of the line scan regulator is selected because, of EHT generator 30, line scan circuit 50, frame scan circuit 40, and video amplifier 60, line scan circuit 50 is the dominant consumer of electrical power, and therefore the largest load on power supply 20.

In normal operation, processor 6 holds shutdown output 13 low. Q4 thus remains off. Error amplifier compares VFB with VREF to generate an error signal at the collector of Q4. The error signal on the collector of Q4 modulates the current from supply rails Vs' and Vs'' through LED 5b of the opto-isolator.

Photo-transistor 5a translates light detected from LED 5b into a feedback signal on feedback input 12 of control device 4. As hereinbefore described, the switching signal on the gate of Q1 is pulse-width modulated as a function of the feedback signal to regulate the voltage on supply rail Vs on the secondary side of the SMPS 20. The voltage on supply rail Vs' derived from secondary winding S2 tracks the voltage on supply rail Vs. The pulse-width of the switching signal effectively determines the amounts of energy transferred from primary side 21 to secondary side 22 by flyback action in T1.

Processor 6 configures the CRT display to operate in a standby mode of operation in response to, for example, a signal from the host computer system. To configure the CRT display to operate in standby mode, processor 6 sets output 13 high. Q4 therefore turns on, thereby bypassing the output of error amplifier 7. The opto-isolator responds by generating a feedback signal at feedback input 12 demanding zero duty cycle from Q1.

The flyback energy stored in the core of T1 decreases in response to the zero duty cycle demand. The voltage on supply rail Vf connected to flyback winding P2 therefore falls to near zero. Control device 4 thus turns off. However, power is maintained to oscillator 1, multiplexor 2, and driver 3 via supply rail Vo by transformer action on forward winding P3. As control device 4 turns off, control output 10 to multiplexor 2 goes low, thereby connecting the output of oscillator 1 to the gate of Q1 via driver 3. Q6 opens in response to control output going low, thereby disconnecting supply input Vf from supply rail Vo.

Oscillator 1 is configured to generate a switching signal having a fixed frequency set to just beyond the audio range of frequencies, at 20kHz, and a fixed reduced pulse-width of 450ns, to switch Q1 on for a short conduction time of 450ns at 50us intervals. The fixed frequency of the switching signal generated by oscillator 1 is significantly lower than the range of line scan frequencies to which the oscillator of control device 4 is synchronised during normal operation. Similarly, the pulse width of the switching signal generated by oscillator 1 is significantly shorter than the shortest pulse length produced by the pulse width modulator of control device 4 during normal operation.

Q1 now alternately opens and closes the current path through T1 in response to the lower frequency, lower pulse width, switching signal from oscillator 1. The flyback energy stored in the core of T1 is now much lower than that stored during normal operation. The reduced flyback action in secondary winding S1 causes the voltage on supply rail Vs to drop from around 75V to typically between 8 and 20V and the voltages on supply rail Vs' from secondary winding S2 to drop proportionately. When the voltage on supply rail Vs''' drops by a sufficient amount, from 12V to typically below 10V, Q3 turns on. Supply rail Vs is therefore connected to the input of voltage regulator 9. The voltage on supply rail Vs'' at the output of regulator 9, typically 5V, is therefore maintained by the reduced voltage on supply rail Vs. Power to processor 6 is thus maintained despite the absence of power to line drive circuit 50, EHT generator 30, frame scan circuit 40, and video amplifier 60. Processor 6 can thus continue to

monitor line and frame sync signals HSYNC and VSYNC and video signals R, G, and B input to the CRT display.

Processor 6 restores normal operation of the CRT display in response to, for example, another signal from the host computer system, indicative of keyboard activity for example. To restore normal operation, processor 6 sends output 12 low, thereby turning Q4 off. The opto-isolator, powered via supply rail Vs'' and D8, therefore configures Q2 to close via D3. Power is thus supplied to control device 4 from supply rail Vm via R1. Control device 4 thus turns on again sending control output 10 high. Q6 closes in response to control output 10 going high, thereby connecting supply input Vf to supply Vo via D9. Multiplexor 2 therefore gates switching signal output 11 back onto the gate of Q2 via driver 3. When supply rail Vs''' reaches typically 10V, Q3 turns off and power on supply rail Vs'' to processor 6 is once again derived from supply rail Vs''' via voltage regulator 9.

A preferred embodiment of the present invention has now been described with reference to a CRT display for a computer system. It will however be appreciated that the present invention is equally applicable to other electrical appliances such as, for example, television receivers. It will also be appreciated that some or all of oscillator 1, multiplexor 2, and driver 3 may be integrated into a single application specific integrated circuit device.

## CLAIMS

1. A controller for a switch mode power supply, the controller comprising: a first oscillator (4) for generating a first pulse signal for actuating a switching device (Q1) of the power supply, the first pulse signal having a first frequency; and a pulse width modulator (12) for receiving a feedback signal indicative of a load on the power supply and for varying the pulse width of the first pulse signal generated by the first oscillator (4) as a function of the feedback signal; characterised in that the controller comprises: a second oscillator (1) for generating a second pulse signal having a second frequency for actuating the switching device (Q1), the second pulse signal having a second frequency lower than the first frequency; and a multiplexor (2) for selectively supplying one of the first pulse signal and the second pulse signal to the switching device (Q1) in response to a control signal to configure the switch mode power supply to operate in a corresponding one of a higher power normal operating mode or a lower power standby mode.

2. A controller as claimed in claim 1, wherein the frequency of the second pulse signal generated by the second oscillator means (1) is greater than 20kHz.

3. A controller as claimed in claim 2, wherein the pulse width of the second pulse signal generated by the second oscillator means (1) is less than 1us.

4. A controller as claimed in claim 2 and claim 3, wherein the frequency of the first pulse signal is in the range 30kHz to 100kHz.

5. A switch mode power supply, comprising: a transformer having a primary winding and at least one secondary winding; a switching device connected to the primary winding of the transformer; and a controller as claimed in any preceding claim connected to the switching device, the feedback signal being derived from the secondary winding of the transformer.

6. Display apparatus comprising: drive means for driving a display device in response to one or more video signals, processor means for controlling the drive means and a switch mode power supply as claimed in claim 5.

**Patents Act 1977**
**Examiner's report to the Comptroller under Section 17 (The Search Report)** -13-

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**Relevant Technical fields**

(i) UK Cl (Edition L ) G3U (UAE9) H2F (FMDRT, FMDRX, FCTV) H4T (TABE, TABF, TADD)

(ii) Int Cl (Edition 5 ) H02M (3/335) H04N (3/185, 5/63)

**Search Examiner**
D C BRUNT

**Databases** (see over)
(i) UK Patent Office

(ii) ONLINE DATABASES: WPI

**Date of Search**
10 SEPTEMBER 1993

**Documents considered relevant following a search in respect of claims** 1-6

| Category (see over) | Identity of document and relevant passages | Relevant to claim(s) |
|---|---|---|
| X | EP 0265322 A1 (THOMSON) - see Figure 2 | 1,5,6 |

| Category | Identity of document and relevant passages | Relevant to claim(s) |
|---|---|---|
| | | |

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X: Document indicating lack of novelty or of inventive step.

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